

15

Abstract

The present invention provides for adjusting the delay time interval of an input signal by controlling the internal register value and internal signal in a semiconductor integrated circuit device, or an external signal. The invention comprises a first gate array 10 for carrying out fine adjustment of the delay time interval of the input signal, capacitances 5 60 to 63 and 70 to 73 connected to the output side of a specified gate in the first gate array via first switching device 40 to 43, a second gate array 20 for carrying out rough adjustment of the delay time interval of the input signal; and a control device 30 that adjusts the delay time interval of the input signal by adjusting the capacitances connected to the output side 10 of a specified gate in the first gate array and the number of gate stages in the second gate array 20.

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